REMARKS

Claims 1-24 are amended to make them more definite and certain and a new claim 25 is added.

1. Claims 1-3, 5-10 and 12, 13, 17, 19, 20, 22 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. patent publication number 2003/0074178 (Sample). The Examiner is respectfully requested to withdraw the rejection of these claims in view of the following comments distinguishing these claims (as amended) over Sample.

Claim 1

Claim 1 recites an apparatus for performing an emulation of an electronic circuit and for transmitting and receiving network packets conveying data relating to the emulation. The apparatus comprises at least one emulation resource mounted on a circuit board and having a network address. A network interface circuit mounted on the circuit board receives (via a network) a packet addressed to an emulation resource and conveying a force command, and a resource interface circuit mounted on the circuit board responds to the force command by setting input signals of the addressed emulation resources to states indicated by data conveyed in the packet. Thus during an emulation network commands conveyed by incoming packets can control states of emulation resource input signals.

Sample (FIG. 11) teaches an emulation system having emulation resources (logic chips 10) mounted on several logic boards 200 installed in slots of a motherboard as illustrated in FIG. 13. As illustrated in FIG. 12, multiplexer boards 400 also installed in the motherboard provide signal paths interconnecting input and output terminals of the logic chips 10 on separate logic boards 200. Thus Sample teaches that multiplexers should route the output signals of resources 10 on one board 200 to input terminals of resources 10 mounted on another board 200. Sample does not teach that interface circuits on the logic boards 200 should control states of input signals to resources 10 in response to force commands conveyed by packets arriving on a network as recited in claim 1.

The Examiner points to paragraphs [0108] and [0122] as teaching the use of network packets to control input signals to resources 10. However, paragraph [0108] teaches that logic boards 200, multiplexer boards 400 and other types of boards installed on a motherboard (FIG. 13) provide various signal paths between the boards, and does not teach that the logic boards 200 receive packets via a network that control states of input signals to their emulation resources 10.

Paragraph [0108] of Sample does teach that a CPU 700 mounted on a separate control board 600 (FIG. 20) has a network (Ethernet) interface, but Sample does not discuss the purpose of the Ethernet connection to CPU 700. In particular Sample does not teach that the logic boards 200 containing the emulation resources 10 have network interfaces that can receive packets arriving via a network. Nor does Sample teach that packets transmitted via the network to CPU 700 control states of emulation resource input signals. Note that the network (Ethernet) interconnection to the CPU 700 mounted on control board 600 does not extend to logic boards 200.

Paragraph [0122] teaches that each logic board 200 (FIG. 20) includes a processor 206 that communicates with CPU 700 on control board 600 via a VME bus interface 222. Paragraph [0122] teaches that processor 206 performs diagnostics, loads configuration data into the logic chips 10 (i.e. programs the logic chips), and transfers data in an out of memory 210 mounted on the logic board (FIG. 11). Nothing in paragraph [0122] or anywhere else in Sample teaches that any device on logic board 200 of FIG. 11 or 20 sets states of input signals to the logic chips 10 during an emulation in response to commands conveyed in packets arriving at the logic board 200 via a network.

Thus Sample fails to teach the subject matter of both the claim 1 (as originally filed and as amended) because Sample fails to teach that an interface circuit on a logic board 200 sets states of input signals of emulation resources 10 in response to packets arriving via a network. Claim 1 as amended also recites that the emulation resources have network addresses and that the packets include destination addresses addressed to the emulation resources. Sample does not teach that emulation resources have network address. Thus the claim 1 (original and as amended) is patentable over Sample.

Claims 2 and 22

Claims 2 and 22 recites that random access memory (RAM) is also mounted on the circuit board, that the resource interface circuit stores data representing states of output signals produced by the at least one emulation resource in the RAM during the emulation, and that the network interface circuit thereafter transmits on the network packets conveying the data stored in the RAM.

Sample's FIG. 20 shows that a logic board 200 includes RAM 226, but while the DRAM is connected to a controller 221, a processor 206 and a VME interface circuit, none of those devices receive packets via a network, and therefore cannot write data conveyed by such packets into DRAM 226 as recited in claims 2 and 22.

The Examiner cites Sample paragraphs [0015], [0189] and [0191] as teaching a RAM mounted on a circuit board with the emulation resources. Paragraph 0015 speaks of programmable logic devices including logic and storage elements, but does not mention a RAM. Paragraphs [0189] and [0191] discuss a memory circuit (FIG. 22a) that includes a RAM 1050. Paragraph [0186] indicates that the "memory circuit" is created by appropriately programming logic devices 10 to implement the memory circuit. Thus the "RAM" 1058 mentioned at paragraph [0191] is within a logic chip 10 of FIG. 11. As discussed above, logic chips 10 communicate with one another through signal paths provided by multiplexer 12 on logic board 200 and with devices on other logic boards through multiplexer cards 420 (FIG. 12). Since the input signals of logic chips 10 are not controlled by data conveyed by network packets, the data written into any "RAM" implemented by a logic chip 10 is not provided by such packets as recited in claims 2 and 22, and Sample does not suggest they could be. Thus claims 2 and 22 (original and as amended) are patentable over Sample.

Claims 3 and 23

Claims 3 and 23 recite that during the emulation the resource interface circuit controls states of inputs signals it transmits to the emulation resource in response to the data conveyed in packets prior to the emulation that is written a the RAM also mounted on the

board. Thus in addition to controlling states of emulation resource input signals in response to data arriving by packets during the emulation (as recited in claim 1), the emulation resource also controls states of emulation resource input signals in response to packet data that was written into an on-board RAM before the emulation began.

For example, the packet data arriving at the circuit board and written into the RAM before the start of the emulation can define the behavior of test signal inputs to the circuit being emulated. The packet data arriving during the emulation can define behavior of output signals of portions of the circuit being emulated by resources that are mounted on other circuit boards. See specification paragraphs [0040] and [0041].

The Examiner cites Sample paragraph [0111] as teaching that a RAM mounted on the circuit board stores data conveyed in packets prior to the emulation as recited in claim 3. However paragraph [0111] discusses an I/O board 300 and a core board 500 (FIG. 16) rather than the logic boards containing emulation resources. Core board 500 contains only cross-connect wiring and no RAM. I/O board 300 does include a RAM 302 which is used to store data for controlling states of input signals to logic chips 310, but Sample does not teach that the data written into RAM 302 comes from packets conveyed to board 300 via a network as recited in claim 3. The data is written into RAM 302 via a conventional processor bus 310 connected to a processor 208 of FIG. 20 on the board (see last five sentences of paragraph [0111]. FIG. 20 shows that the processor 206 communicates via buses and control and interrupt lines with a VME interface 222 and a controller 221. Nothing in Sample indicates that processor 206 receives the data it writes into RAM 302 of FIG. 16 from network packets arriving at board 300. Board 300 does not have a network connection.

Thus claims 3 and 23 (both original and as amended) are patentable over Sample.

Claims 5-8, 10, 12, 13, 17 and 20

Claims 5-8, 10, 12, 13, 17 and 20 (original and as amended) are patentable over Sample for reasons indicated above in connection with their parent claim 1.

Claim 9

Claim 9 recites that the emulation resource comprises a plurality of programmable logic devices (PLDs), that the resource interface circuit generates at least one clock signal, and that a clock bus connected between the resource interface circuit and each PLD delivers edges of the at least one clock signal to each PLD for clocking logic circuits within the PLDs during the emulation. Claim 9 further recites that the resource interface circuit generates edges of the at least one clock signal in response to packets received via the network. See the applicant's specification paragraph [0048].

The Examiner cites Sample paragraphs [0105] and [0106] as teaching the subject matter of claim 9, however, those paragraphs do not mention anything about packets conveyed by a network initiating edges of clock signals generated by interface circuit mounted on Sample's logic boards 200. Paragraph [0106] instead teaches that the clock signals delivered to PLDs 10 should be generated by a chip 204 in the logic boards 200 (FIG. 11) wherein edges of the clock signals are controlled not by packets delivered to the logic boards 200 but by edges of master "CLOCK IN" signals 218 supplied as inputs to boards 200. Claim 19 also recites that the resource interface circuit generates edges of the at least one clock signal in response to packets received via a network. Nothing in Sample teaches that packets delivered to logic boards 200 provide any control over timing of clock signal edges generated locally on the logic boards 200. Hence claims 9 and 19 (both original and as amended) are patentable over Sample.

2. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sample in view of US patent 6,034,538 (Abramovici). The Examiner is respectfully requested to withdraw the rejection in view of the following comments distinguishing claim 4 over the combination of Sample and Abramovici.

The Examiner cites only Sample and not Abramovici as teaching the underlying subject matter of claim 1. However as discussed above, Sample fails to teach the underlying subject matter of claim 1. Claim 4 (original and as amended) is therefore patentable over the combination of Sample and Abramovici.

The Examiner further cites Abramovici as teaching a host computer that writes configuration data (programming data) for emulation resources (FPGAs) in a RAM 24 (FIG 2). Abramovici does not directly say what writes the programming data into RAM 24 although col. 4, lines 57-59 seem to suggest that it could be written into the RAM by a host processor and/or "reconfigurable" hardware. In any case, claim 4 does not recite storing FPGA programming data in a RAM; it recites that resource interface circuit supplies data conveyed by packets received via the network as the input programming data to an emulation resource. Abramovici teaches nothing about using data conveyed in packets to program emulation resources as recited in claim 4, and indeed makes no mention of packets or networks for any purpose.

Claim 4 (original and as amended) is therefore patentable over the combination of Sample and Abramovici.

3. Claims 11 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sample in view of the paper entitled "AnyBoard: An FPGA-based, Reconfigurable System" (Morris). The Examiner is respectfully requested to withdraw the rejection of these claims in view of the following comments distinguishing them over the combination of Sample and Morris.

Claims 11 and 21

The Examiner cites only Sample and not Morris as teaching the underlying subject matter of claim 1. However since Sample fails to teach the underlying subject matter of claim 1 for the reasons discussed above, and since Morris also fails to teach them, claims 11 and 21 are patentable over the combination of Sample and Morris.

Claims 11 and 21 further recite an oscillator mounted on the circuit board containing the emulation resources for generating a primary clock signal, wherein the resource interface circuit generates edges of a clock signal supplied to the emulation resources in

response to edges of the primary clock signal. Sample's primary clock signals are not generated on the logic boards 200 containing the emulation resources but rather on a separate control board 600 (FIG. 19). The Examiner cites Morris as teaching that an oscillator can be used to clock signals for clocking emulation resources even though Sample also teaches to use an oscillator (OSC) on board 600 (FIG. 19) as a source for the primary clock signals. In any case one would not be motivated use a separate oscillator on each of Sample's logic boards 200 to generate the primary clock signal required by all logic chips because in order for Sample's emulator to function properly, all of the clock signals on all of the logic boards must be synchronized to the same clock signal. If each logic board 200 were to use a separate oscillator as the source of its clock signals, synchronicity between the logic chips on the separate boards 200 would be lost and Sample's emulator would fail to operate properly. Thus nothing in Sample and Morris would motivate one of skill in the art to provide an oscillator on each logic board for use as a clock signal source. Claims 11 and 21 (both original and as amended) are therefore patentable over the combination of Sample and Morris.

4. Claims 14-16, 18 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sample in view of the paper "Routing Architecture and Layout Synthesis for Multi-FPGA Systems" (Khalid). The Examiner is respectfully requested to withdraw the rejection of these claims in view of the following comments distinguishing these claims over the combination of Sample and Khalid.

Claims 14, 15 and 24

The Examiner cites only Sample and not Khalid as teaching the underlying subject matter of claim 1. However since Sample fails to teach the underlying subject matter of claim 1 for the reasons discussed above, and since Khalid also fails to teach them, claims 14, 15 and 24 (both original and as amended) are patentable over the combination of Sample and Khalid.

Claims 16 and 18

The Examiner cites only Sample and not Khalid as teaching the underlying subject matter of claim 1. However since Sample fails to teach the underlying subject matter of claim 1 for the reasons discussed above, and since Khalid also fails to teach them, claim 16 is patentable over the combination of Sample and Khalid.

Claims 16 and 18 further recite the resource interface circuit controls a plurality of switches interconnecting PLDs or FPGAs to RAMs in response to data conveyed in packets received via the network. The Examiner points to Khalid section 3 as teaching this, but Khalid section 3 teaches only various hard wire signal paths for interconnecting PLDs. Neither Khalid nor Sample teaches or suggests using data conveyed by network packets to control switches interconnecting RAMs to PLD's or FPGAs as recited in claim 16 and 18. Claims 14 and 15 (both original and as amended) are therefore patentable over the combination of Sample and Khalid.

In view of the foregoing amendments and remarks, it is believed the application is in condition for allowance. Notice of Allowance is therefore respectfully requested.

Respectfully submitted,

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Penelope Stockwell